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10/080,440	02/22/2002	Ashish Gupta	10019865-1	8447

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EXAMINER	
SHAH, SAUMIL R	

ART UNIT	PAPER NUMBER
2186	3

DATE MAILED: 11/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,440	GUPTA ET AL.	
	Examiner	Art Unit	
	Saumil Shah	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *12-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-11, drawn to access a plurality of memories in an interleaved manner wherein at least one map table is provided which includes a plurality of entries, each entry including a plurality of entry items, each entry item identifying one of the memories. The entry items are then identified using three sets of bits from a logical address, classified in class 711, subclass 157.

   II. Claims 12-28, drawn to access a plurality of memories in an interleaved manner wherein at least one map table is provided which has a base number of entry items in each entry where this base number identifies the number of ways of interleaving memories. Each entry item identifies one of the memories. (Note especially claim 12, lines 21-22 and claim 19, lines 12-14), classified in class 711, subclass 157.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP §

806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because there need not be a base number of entry items in each entry such that this base number identifies the number of interleaved memories. It could have as many items per entry as is required independent of the number of ways of interleaving. The subcombination has separate utility such as having a base number of items in each entry in the map table so that the number of ways of interleaving can be identified directly from the number of items per entry in the map table.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Jeff A. Holmen on 11/03/2003 a provisional election was made without traverse to prosecute the invention of group I, claims 1-11. Affirmation of this election must be made by applicant in replying to this Office action. Claims 12-28 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

6. Applicant is requested to update the first page of the specification with the serial number of the copending U.S. application (Gupta et al., Appl No. 10/080,739).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4, 7, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lunteren (US Patent No. 6,381,668).

a. With regard to claims 1, Lunteren discloses a method of accessing a plurality of memories in an interleaved manner using a logical address space (note column 3, lines 63-65), the method comprising:

providing at least one map table, the at least one map table including a plurality of entries (note column 4, lines 3-5 where mapping means teaches a map table), each entry including a plurality of entry items, each entry item identifying one of the memories (note figs 3B and 3C in which the table in 3C has multiple entries and they correspond to one of the banks); and

accessing the memory identified by the first entry item (note it is well known in the art that the mapped memory would then be accessed corresponding to the address).

However, Lunteren differs in the following features of claim 1:

i. Contiguous logical address space

ii. receiving a first logical address, the first logical address including a plurality of address bits (note column 5, lines 49-52), the plurality of address bits including a first set of address bits corresponding to a first set of entries in the at least one map table (note column 5, lines 51-52 where Y can be considered to be the first set of address bits. Further note column 6, lines 3-6 where X and Y portions are used to identify the bank of memories);

iii. identifying a first entry in the first set of entries based on the first set and a second set of the address;

iv. identifying a first entry item in the first entry based on a third set of the address bits; bits (note column 6, lines 3-6 where X and Y portions are used to identify the bank of memories which is the "first set of entries". Further note, column 8, lines 29-31, where any combination of bits except Y is used to identify the entry and entry item) and

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a contiguous logical address space. Note figure 1B where the virtual address space is shown to map into the physical address space and it is obvious that the entire virtual space is mapped and that it would be contiguous else the purpose of using virtual addresses would be defeated. So it would have been obvious to use a contiguous logical address space since it

would make the memory interleaving transparent to the user. Further, it would have been obvious to use another combination of bits from the address to map to the entry item in the set of entries since the final result is that an entry item is selected from a set of entries using the bits of the address.

b. With regard to claim 2, Lunteren discloses the method of claim 1, wherein the first, second, and third sets of address bits are non-overlapping (note column 8, lines 14-16).

c. With regard to claim 3, Lunteren discloses the method of claim 1, wherein the first, second, and third sets of address bits are each separated from one another by a plurality of other bits (note column 8, lines 11-14 where the third set of bits could be any set of bits excluding those in X and Y).

d. With regard to claim 4, Lunteren discloses the method of claim 1, wherein the first set of address bits include more significant bits than the second set of address bits, and wherein the second set of address bits include more significant buts than the third set of address bits (note column 8, lines 28-35 where the bits could be in any order of significance and so this particular format of bits is one of the possible configurations).

e. With regard to claim 6, Lunteren discloses the method of claim 1, and further comprising:

storing a plurality of memory offset values in the at least one map table;

identifying one of the memory offset values based on the first logical address; and

wherein the memory identified by the first entry item is accessed at a memory location based at least in part on the identifies memory offset value (note figure 4A where the rightmost table contains entry items which represent offset values in the memory. Further note, column 5, lines 36-38 where the entry items is said to represent a block).

f. With regard to claim 7, Lunteren et al disclose the method of claim 1, wherein the at least one map table is organized into a plurality of rows and a plurality of columns, and wherein each row corresponds to one of the plurality of entries and each column within a row corresponds to one of the plurality of entry items (note figure 4A, rightmost table where the map table consists of a plurality of rows which form entry items and plurality of columns which form entries and that it has been well known in mathematics that the matrix can be inverted so that rows now become columns and columns become rows).

g. With regard to claim 11, Lunteren disclose the method of claim 1, wherein the memories each include at least one memory segment, the memory segments organized into groups, the memory segments in each groups having a uniform size, and wherein each entry in the at least one map table corresponds to one of the groups of memory segments (note figure 4A where the rightmost table has columns that corresponds to banks of memory blocks which teaches "groups of memory segments").

2. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lunteren (US Patent No. 6,381,668) in view of Grossier (US Patent No 6,553,478).

a. With regard to claim 6, Lunteren discloses the subject matter of claim 1. However, it fails to mention the following feature

method of claim 1 wherein the first logical address is a processor address.

Grossier discloses a system in which the logical address is a processor address (note column 3, lines 2-3 and lines 22-23 where the processor consists of an address controller which outputs an address to the system memory and can hence be considered a processor address).

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a processor address as a logical address since that would allow the processor to access the memory without extra processing to calculate the physical memory address.

2. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lunteren (US Patent No. 6,381,668) in view of Douglas et al (US Patent No 6,480,943).

a. With regard to claim 8, Lunteren discloses the subject matter of claim 1 except:

i. providing a multi-bit mask value;

ii. providing a plurality of multi-bit match values;

iii. extracting the first set of address bits from the first logical address using the multi-bit mask value; and

iv. comparing the extracted first set of address bits to the plurality of multi-bit match values to identify a match.

Douglas et al teach a method comprising:

providing a multi-bit mask value (note figure 5, 510);

providing a plurality of multi-bit match values (note column 7, lines 63-64 where the comparator is a "multi-bit match value");

extracting the first set of address bits from the first logical address using the multi-bit mask value (note figure 5, 510 where the mask is used to extract address bits and compare with comparator); and

comparing the extracted first set of address bits to the plurality of multi-bit match values to identify a match (note column 7, lines 65-67 where determining a specific row is done by matching value masked with comparator).

Hence, it would have been obvious to one of ordinary skill at the time the invention was made to have used a mask value and a comparator value since that would reduce the size of the comparator required to match the values of the masked value and the comparator value. It would additionally ease the process of mapping addresses to a specific entry item in the map table.

b. With regard to claim 9, Lunteren discloses the subject matter of claim 1 except:

i. providing at least one multi-bit mask value;

ii. providing a plurality of multi-bit match values;

iii. extracting the second set of address bits from the first logical address using the at least one multi-bit mask value;

iv. comparing the extracted second set of address bits to the plurality of multi-bit match values; and

v. wherein the first entry in the first set of entries is identified based at least in part on the comparison of the extracted second set of address bits to the plurality of multi-bit match values

Douglas et al teach a method comprising:

providing at least one multi-bit mask value(note figure 5, 510);

providing a plurality of multi-bit match values (note column 7, lines 63-64 where the comparator is a "multi-bit match value");

extracting the second set of address bits from the first logical address using the at least one multi-bit mask value (note column 7, lines 2-6-27 where the mask is used to mask out bits not required to determine row and so it could be used to extract the second set of address bits as it is used to identify the entry);

comparing the extracted second set of address bits to the plurality of multi-bit match values (note column 7, lines 65-67 where determining a specific row is done by matching value masked with comparator); and

wherein the first entry in the first set of entries is identified based at least in part on the comparison of the extracted second set of address bits to the plurality of multi-bit match values (note column 7, lines 65-67 where determining a specific row is done by matching value masked with comparator and entry is taught by a row).

Hence, it would have been obvious to one of ordinary skill at the time the invention was made to have used a mask value and a comparator value since that would reduce the size of the comparator required to match the values of the

masked value and the comparator value. It would additionally ease the process of mapping addresses to a specific entry item in the map table.

c. With regard to claim 10, Lunteren discloses the subject matter of claim 1 except:

i. providing a plurality of multi-bit mask value;

ii. providing a plurality of multi-bit match values;

iii. selecting one of the plurality of multi-bit mask values based on a desired interleave entry size

iv. extracting the second set of address bits from the first logical address using the selected multi-bit mask value;

v. comparing the extracted second set of address bits to the plurality of multi-bit match values; and

vi. wherein the first entry in the first set of entries is identified based at least in part on the comparison of the extracted second set of address bits to the plurality of multi-bit match values

Douglas et al teach a method comprising:

providing a plurality of multi-bit mask value(note figure 5, 510 and it is obvious that if there are multiple interleave configurations possible then multiple mask values will be used. Further note figures 3,4 which shows different interleave configurations);

providing a plurality of multi-bit match values (note column 7, lines 63-64 where the comparator is a "multi-bit match value");

selecting one of the plurality of multi-bit mask values based on a desired interleave entry size (it is obvious that if there are multiple interleave configurations possible then multiple mask values will be used. Further note figures 3,4 which shows different interleave configurations and so the selection of the mask value would depend on the interleave entry size)

extracting the second set of address bits from the first logical address using the selected multi-bit mask value (note column 7, lines 2-6-27 where the mask is used to mask out bits not required to determine row and so it could be used to extract the second set of address bits as it is used to identify the entry);

comparing the extracted second set of address bits to the plurality of multi-bit match values (note column 7, lines 65-67 where determining a specific row is done by matching value masked with comparator); and

wherein the first entry in the first set of entries is identified based at least in part on the comparison of the extracted second set of address bits to the plurality of multi-bit match values (note column 7, lines 65-67 where determining a specific row is done by matching value masked with comparator and entry is taught by a row).

Hence, it would have been obvious to one of ordinary skill at the time the invention was made to have used multiple mask values and comparator values since that would reduce the size of the comparator required to match the values of the masked value and the comparator value. It would also be important to use different mask values for different interleave entry sizes so that groups can be

distinguished between efficiently. It would additionally ease the process of mapping addresses to a specific entry item in the map table.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saumil Shah whose telephone number is 703-305-8786. The examiner can normally be reached on 9:00 AM to 5:30 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Saumil Shah
Examiner
Art Unit 2186

18th November 2003

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER